

CLAIMS

We claim:

- 1 1. A circuit for synchronously exchanging
2 bidirectional data, comprising:
3 at least two driving entities connected to a bus
4 for sending and receiving data to each other, said at
5 least two driving entities each comprising a master
6 latch having scan-in port for receiving a scan test
7 vector;
8 a swapper circuit electrically connected to said
9 bus at a connection point between said at least two
10 driving entities, said swapper circuit for capturing
11 data simultaneously traveling in opposite directions on
12 said bus and passing said captured data back onto said
13 bus avoiding collision of the data; and
14 a capture latch at either end of said bus for
15 capturing received data.
- 1 2. A circuit for synchronously exchanging bidirectional
2 data as recited in claim 1 further comprising:
3 a slave latch having an input connected to an
4 output of said master latch, said slave latch having a
5 scan-out port for outputting the scan test vector.
- 1 3. A circuit for synchronously exchanging
2 bidirectional data as recited in claim 1 wherein said
3 at least two driving entities comprise:
4 a tri-state circuit connected to said master latch
5 for driving data output from said master latch onto
6 said bus.

1 4. A circuit for synchronously exchanging
2 bidirectional data as recited in claim 1 wherein said
3 swapper circuit comprises:
4 a first latch and tri-state circuit pair connected
5 to said bus for providing a path for data traveling on
6 said bus in one direction; and
7 a second latch and tri-state circuit pair
8 connected to said bus for providing a path for data
9 traveling on said bus in an opposite direction.

1 5. A circuit for synchronously exchanging
2 bidirectional data as recited in claim 2 wherein said
3 first latch and said second latch of said swapper
4 circuit are connected to receive a system clock and a
5 scan clock.

1 6. A circuit for synchronously exchanging bidirectional
2 data as recited in claim 2 wherein a plurality of said
3 circuits for synchronously exchanging bidirectional
4 data are connected together with said scan-out port of
5 a first circuit connected to a scan-in port of a second
6 circuit.

1 7. A circuit for synchronously exchanging bidirectional
2 data, comprising:
3 at least two driving entities connected to a bus
4 for sending and receiving data to each other, said at
5 least two driving entities each comprising a master
6 latch having scan-in port for receiving a scan test
7 vector and a data output port connected to said bus;
8 a swapper circuit electrically connected to said

17 said master latch, said slave latch having a scan-out
18 port for outputting the scan test vector;
19 connecting said driving entities, said swapper and
20 said capture latch and said slave latch to a plurality
21 of synchronous clocks;
22 inputting a scan test vector into said scan-in
23 port;
24 enabling ones of said synchronous clocks to move
25 said scan test vector through said circuit for one of a
26 plurality of test patterns; and
27 reading data output from said scan-out port.

1 14. A method for scan testing a circuit for
2 synchronously exchanging bidirectional data as recited
3 in claim 13 wherein said test pattern is a
4 unidirectional test pattern moving said scan test
5 vector from one of an X direction to a Y direction and
6 a Y direction to an X direction.

1 15. A method for scan testing a circuit for
2 synchronously exchanging bidirectional data as recited
3 in claim 13 wherein said test pattern is a bi-
4 directional test pattern moving a first scan test
5 vector from an X direction to a Y direction and a
6 second test vector from a Y direction to an X
7 direction.

1 16. A method for scan testing a circuit for
2 synchronously exchanging bidirectional data as recited
3 in claim 13 further comprising the step of:
4 connecting said scan-out port to a scan in port of
5 a next one of said circuits for synchronously

6 exchanging bidirectional data, such that a plurality of
7 said circuits are connected together in series.

1 17. A method for scan testing a circuit for
2 synchronously exchanging bidirectional data as recited
3 in claim 16 wherein said test pattern is one of an "S"
4 test pattern and a "Z" test pattern.

6630-33660